Our Docket No: 42390P7143

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:		
Jassowski	Examiner:	Zarneke, David A.
Application No: 09/475,643	Art Unit:	2891
Filed: December 30, 1999		
For: Optimized Driver Layout for Integrated Circuits with Staggered Bond Pads		

RESPONSE TO NOTICE OF NON-COMPLIANT APPEAL BRIEF

Mail Stop Appeal Brief
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

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Date of Deposit: March 24, 2006
Name of Person Mailing Correspondence: Krista Mathieson

Krista Mathieson — Signature
March 24, 2006 — Date

In response to the Notice of Non-Compliant Appeal Brief mailed on March 8, 2006, please find the amended Appeal Brief enclosed herewith to replace the Appeal Brief submitted on January 12, 2006.

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: March 24, 2006

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Our Docket No.: 42390P7143

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:	)	
	)	
Michael A. Jassowski	)	Examiner: Zarneke, David A.
	)	
Application No: 09/475,643	)	Art Unit: 2891
	)	
Filed: December 30, 1999	)	
	)	
For: Optimized Driver Layout for Integrated Circuits with Staggered Bond Pads	)	

Mail Stop: Appeal Brief - Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF
IN SUPPORT OF APPELLANT'S APPEAL
TO THE BOARD OF PATENT APPEALS AND INTERFERENCES

Sir:

Applicant (hereinafter "Appellant") hereby submits this Appeal Brief (hereinafter "Brief") in support of its appeal from a final decision by the Examiner, mailed August 17, 2005 in the above-referenced Application. Appellant respectfully requests consideration of this appeal by the Board of Patent Appeals and Interferences (hereinafter "Board") for allowance of the above-captioned patent application.

An oral hearing is not desired.

TABLE OF CONTENTS

I. REAL PARTY IN INTEREST

The invention is assigned to Intel Corporation of 2200 Mission College Boulevard, Santa Clara, California 95052.

II. RELATED APPEALS AND INTERFERENCES

To the best of Appellant's knowledge, there are no appeals or interferences related to the present appeal that will directly affect, be directly affected by, or have a bearing on the Board's decision.

III. STATUS OF THE CLAIMS

Claims 1, 3, 5-8, 23-27 and 35-48 are currently pending in the above-referenced application. No claims have been allowed.

IV. STATUS OF AMENDMENTS

Claims 1, 3, 5-8, 23-27 and 35-48 are currently pending in the subject application. These claims were finally rejected in a final Office Action mailed August 17, 2005 (hereinafter "Office Action"). The Examiner confirmed the final rejection of these claims in an Advisory Action mailed November 29, 2005.

In response to the Office Action rejecting claims 1, 3, 5-8, 23-27 and 35-48 under 35 U.S.C. §§102(b) and 103(a), Appellant filed a Response After Final pursuant to 37 C.F.R. § 1.116 on November 15, 2005. Subsequently, an Advisory Action was mailed on November 29, 2005 maintaining all rejections in the final Office Action. In response, Appellant filed a timely Notice of Appeal on November 15, 2005. A copy of all claims on appeal is attached hereto as the Appendix of Claims.

Appellant respectfully traverses each of the grounds of rejection.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

According to one embodiment, a semiconductor device is disclosed. The semiconductor includes a die that has a first edge and a core. The semiconductor device further includes a plurality of bond pads that are configured in a staggered array between the first edge and the core. The staggered array includes an inner ring and an outer ring of bond pads. The semiconductor device also includes a first plurality of driver cells which are located between the first edge and the plurality of bond pads, and a second plurality of driver cells which are located between the plurality of bond pads and the core. (see Specification at page 5, line 3 – page 6, line 20).

According to another embodiment, a semiconductor device is disclosed. The semiconductor device includes a die that has a first edge and a core. The semiconductor device further includes a plurality of bond pads that are configured in an array between the first edge and the core. The semiconductor device also includes a first plurality of driver cells that are located between the first edge and the plurality of bond pads, and a second plurality of driver cells that are located between the plurality of bond pads and the core. The semiconductor device further includes a plurality of conductive interconnects to couple each of plurality of pre-driver cells to one of the first and second pluralities of driver cells. At least one conductive interconnects is disposed on a layer other than a layer. (see Specification at page 5, line 3 – page 6, line 20).

According to another embodiment, a system is disclosed. The system includes a lead frame and a die that is coupled to the lead frame. The die has a first edge, a core and a plurality of bond pads. The plurality of bond pads are configured in a staggered array between the first edge and the core. The staggered array includes an inner ring and an outer ring of bond pads. The die further includes a first plurality of driver cells that are

located between the first edge and the plurality of bond pads, and a second plurality of driver cells that are located between the plurality of bond pads and the core. (see Specification at page 5, line 3 – page 6, line 20).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claim 1 stands rejected under 35 U.S.C. §102(b) as being anticipated by Hayashi, et al., U.S. Patent No. 5,581,109 (hereinafter "Hayashi").

Claims 1, 3, 5, 6, 44, 45, 47 and 48 stand rejected under 35 U.S.C. §102(e) as being anticipated by Hiraga, et al., U.S. Patent No. 6,091,089 (hereinafter "Hiraga").

Claim 44 stands rejected under 35 U.S.C. §102(b) as being anticipated by Pendse, et al., U.S. Patent No. 5,818,114 (hereinafter "Pendse").

Claims 3, 5-8, 23-27 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Hayashi.

Claims 3, 5-8, 23-27 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Pendse.

Claims 7, 8 and 23-27 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Hiraga.

Claims 35-43 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Hayashi.

Claims 35-43 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Pendse in view of Hayashi.

Claims 35-43 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Hiraga in view of Hayashi.

Claims 45-48 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Pendse.

Claim 46 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Hiraga in view of Pendse.

VII. ARGUMENT

A. THE PENDING CLAIMS WERE IMPROPERLY REJECTED UNDER 35 U.S.C. § 102(B) BECAUSE HAYASHI DOES NOT TEACH OR REASONABLY SUGGEST A PLURALITY OF BOND PADS CONFIGURED IN A STAGGERED ARRAY BETWEEN THE FIRST EDGE AND THE CORE, WHEREIN THE STAGGERED ARRAY INCLUDES AN INNER RING AND AN OUTER RING OF BOND PADS

Claim 1 stands rejected under 35 U.S.C. §102(b) as being anticipated by Hayashi, as stated in the Office Action. Appellant respectfully submits that Hayashi does not teach or reasonably suggest the claimed invention for at least the reasons set forth below.

Claim 1 recites:

> A semiconductor device, comprising:
> a die having
> a first edge;
> a core;
> a plurality of bond pads configured in a staggered array between the first edge and the core, wherein the staggered array includes an inner ring and an outer ring of bond pads;
> a first plurality of driver cells located between the first edge and the plurality of bond pads; and
> a second plurality of driver cells located between the plurality of bond pads and the core.
> (emphasis provided)

Hayashi discloses that "FIG. 10 shows a modified configuration of the semiconductor device . . . in which the bonding pads are *arranged in a form of two lines*." (col. 9, lines 59-63; emphasis provided). Appellant respectfully disagrees with the Examiner's assertion the bonding pads in figure 10 of Hayashi are a staggered array including an inner and an outer ring of bond pads. (see the Office Action at page 5, lines 3-5). Two lines of bonding pads are not the same as having an inner and outer ring of staggered bonding pads, as recited by claim 1. Additionally, Hayashi would not have been motivated to modify the two lines of bonding pads to form an inner and outer ring.

This is because Hayashi states that the problem to be fixed is the "*size-increasing of the semiconductor device*" and the way to solve this problem is for "*the bonding pads to be arranged in a plural number of lines* outside the I/O cell circuits", and not in inner and outer rings. (col. 2, lines 1-8; emphasis provided) Accordingly, Appellant respectfully submits that claim 1 and its dependant claims are patentable over Hayashi.

B. THE PENDING CLAIMS WERE IMPROPERLY REJECTED UNDER 35 U.S.C. § 102(E) BECAUSE HIRAGA DOES NOT TEACH OR REASONABLY SUGGEST A PLURALITY OF BOND PADS CONFIGURED IN A STAGGERED ARRAY BETWEEN THE FIRST EDGE AND THE CORE, WHEREIN THE STAGGERED ARRAY INCLUDES AN INNER RING AND AN OUTER RING OF BOND PADS

Claims 1, 3, 5 and 6 stand rejected under 35 U.S.C. §102(e) as being clearly anticipated by Hiraga, as stated in the Office Action. Appellant respectfully submits that Hiraga does not teach or reasonably suggest the claimed invention for at least the reasons set forth below.

Claim 1 recites:

> A semiconductor device, comprising:
> a die having
> a first edge;
> a core;
> a plurality of bond pads configured in a staggered array between the first edge and the core, wherein the staggered array includes an inner ring and an outer ring of bond pads;
> a first plurality of driver cells located between the first edge and the plurality of bond pads; and
> a second plurality of driver cells located between the plurality of bond pads and the core.
> (emphasis provided)

Hiraga discloses "[a] semiconductor integrated circuit device [that] has a semiconductor chip, on which are formed a plurality of input/output circuits and input/output pads individually connected." (Abstract, lines 1-4). Hiraga further discloses that "*input/output pads 5 [are] connected to the input/output circuits . . . arranged in a single row*" (col. 4, lines 4-6; emphasis provided) and the single row is "*the innermost row.*" (col. 4, lines 35-36; emphasis provided). Hiraga further discloses that ". . .

input/output pads 6 and 7 are arranged in a staggered arrangement on both sides of a row of input/output circuits." (col. 4, lines 64-66; emphasis provided).

In contrast, claim 1, in pertinent part, recites "a plurality of bond pads configured in a staggered array between the first edge and the core, wherein the staggered array includes an inner ring and an outer ring of bond pads." (emphasis provided). The Examiner asserts that "Hiraga teaches the plurality of bond pads [5 & 6] [are] configured in a staggered array including an inner ring [5] and an outer ring [6] of bond pads." (Office Action, page 7, lines 3-5). Appellant respectfully disagrees with the Examiner's characterization of Hiraga. In fact, Hiraga teaches that input/output pads 6 and 7 are the pads in the staggered arrangement and not pads 5 and 6. (col. 4, lines 64-66). Nowhere in Hiraga is it taught or reasonably suggested that input/output pads 5 and 6 are in a staggered arrangement. In addition, pads 6 and 7 are not configured in an inner and outer ring. Accordingly, Hiraga does not teach or reasonably suggest "a plurality of bond pads configured in a staggered array between the first edge and the core, wherein the staggered array includes an inner ring and an outer ring of bond pads", as recited by claim 1. (emphasis provided). Appellant respectfully submits that claim 1 and its dependant claims are patentable over Hiraga.

C. THE PENDING CLAIMS WERE IMPROPERLY REJECTED UNDER 35 U.S.C. § 102(B) BECAUSE PENDSE DOES NOT TEACH OR REASONABLY SUGGEST A PLURALITY OF BOND PADS CONFIGURED IN A STAGGERED ARRAY BETWEEN THE FIRST EDGE AND THE CORE, WHEREIN THE STAGGERED ARRAY INCLUDES AN INNER RING AND AN OUTER RING OF BOND PADS

Claim 44 stands rejected under 35 U.S.C. §102(b) as being anticipated by Pendse, as stated in the Office Action. Appellant respectfully submits that Pendse does not teach or reasonably suggest the claimed invention for at least the reasons set forth below.

Claim 44 recites:

> A system comprising:
> a lead frame;
> a die coupled to the lead frame, the die having
> a first edge;
> a core;
> a plurality of bond pads configured in a staggered array between the first edge and the core, wherein the staggered array includes an inner ring and an outer ring of bond pads
> a first plurality of driver cells located between the first edge and the plurality of bond pads and
> a second plurality of driver cells located between the plurality of bond pads and the core.
> (emphasis provided)

Pendse discloses an ". . . I/O pad structure and layout methodology . . ." in which "*the pad layout . . . entails the use of two rows of pads* on the chip periphery as opposed to the more conventional single row . . . arrangement." (Abstract, lines 1-7; emphasis provided).

In contrast, claim 44, in pertinent part, recites "a plurality of bond pads configured in a staggered array between the first edge and the core, wherein the staggered array includes an inner ring and an outer ring of bond pads." (emphasis provided). Pendse discloses *two rows of pads*; however, Pendse fails to teach or reasonably suggest that the

pads are configured in a staggered array and in an inner and outer ring, as recited by claim 44. Accordingly, Appellant respectfully submits that claim 44 and its dependant claims are patentable over Pendse.

D. THE PENDING CLAIMS WERE IMPROPERLY REJECTED UNDER 35 U.S.C. § 103(A) BECAUSE HAYASHI DOES NOT TEACH OR REASONABLY SUGGEST THE CLAIMED INVENTION

Claims 35-43 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Hayashi, as stated in the Office Action.

Claim 35 contains limitations similar to those of claim 1. Accordingly, as previously discussed with regard to claim 1 in issue A (pages 8-9), Appellant submits that claim 35 and its dependent claims are patentable over Hayashi.

E. THE PENDING CLAIMS WERE IMPROPERLY REJECTED UNDER 35 U.S.C. § 103(A) BECAUSE PENDSE IN VIEW OF HAYASHI NEITHER INDIVIDUALLY NOR WHEN COMBINED IN ANY COMBINATION TEACHES OR REASONABLY SUGGESTS THE CLAIMED INVENTION

Claims 35-43 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Pendse in view of Hayashi, as stated in the Office Action.

Claim 35 contains limitations similar to those of claim 1. Accordingly, as previously discussed with regard to claim 44 in issue C (pages 12-13), Appellant submits that claim 35 and its dependent claims are patentable over Pendse in view of Hayashi.

F. THE PENDING CLAIMS WERE IMPROPERLY REJECTED UNDER 35 U.S.C. § 103(A) BECAUSE HIRAGA IN VIEW OF HAYASHI NEITHER INDIVIDUALLY NOR WHEN COMBINED IN ANY COMBINATION TEACHES OR REASONABLY SUGGESTS THE CLAIMED INVENTION

Claims 35-43 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Hiraga in view of Hayashi, as stated in the Office Action.

Claim 35 contains limitations similar to those of claim 1. Accordingly, as previously discussed with regard to claim 1 in issue B (pages 10-11), Appellant submits that claim 35 and its dependent claims are patentable over Hiraga in view of Hayashi.

G. THE PENDING CLAIMS WERE IMPROPERLY REJECTED UNDER 35 U.S.C. § 103(A) BECAUSE HAYASHI DOES NOT TEACH OR REASONABLY SUGGEST THE CLAIMED INVENTION

Claims 3, 5-8, 23-27 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Hayashi, as stated in the Office Action.

Claims 3, 5-8, 23-27 depend from independent claim 1, and thus include all the limitations of the independent claims from which they depend. Accordingly, as previously discussed with regard to claim 1 in issue A (pages 8-9), claims 3, 5-8, 23-27 are patentable over Hayashi.

H. THE PENDING CLAIMS WERE IMPROPERLY REJECTED UNDER 35 U.S.C. § 103(A) BECAUSE PENDSE DOES NOT TEACH OR REASONABLY SUGGEST THE CLAIMED INVENTION

Claims 3, 5-8, 23-27 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Pendse, as stated in the Office Action.

Claims 3, 5-8, 23-27 depend from independent claim 1, and thus include all the limitations of the independent claims from which they depend. Accordingly, as previously discussed with regard to claim 1 in issue A (pages 8-9), claims 3, 5-8, 23-27 are patentable over Pendse.

I. THE PENDING CLAIMS WERE IMPROPERLY REJECTED UNDER 35 U.S.C. § 103(A) BECAUSE HIRAGA DOES NOT TEACH OR REASONABLY SUGGEST THE CLAIMED INVENTION

Claims 7, 8 and 23-27 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Hiraga, as stated in the Office Action.

Claims 7, 8 and 23-27 depend from independent claim 1, and thus include all the limitations of the independent claims from which they depend. Accordingly, as previously discussed with regard to claim 1 in issue B (pages 10-11), claims 7, 8 and 23-27 are patentable over Hiraga.

J. THE PENDING CLAIMS WERE IMPROPERLY REJECTED UNDER 35 U.S.C. § 103(A) BECAUSE PENDSE DOES NOT TEACH OR REASONABLY SUGGEST THE CLAIMED INVENTION

Claims 45-48 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Pendse, as stated in the Office Action.

Claims 45-48 depend from independent claim 44, and thus include all the limitations of the independent claims from which they depend. Accordingly, as previously discussed with regard to claim 44 in issue C (pages 12-13), claims 45-48 are patentable over Pendse.

K. THE PENDING CLAIMS WERE IMPROPERLY REJECTED UNDER 35 U.S.C. § 103(A) BECAUSE HIRAGA IN VIEW OF PENDSE NEITHER INDIVIDUALLY NOR WHEN COMBINED IN ANY COMBINATION TEACHES OR REASONABLY SUGGESTS THE CLAIMED INVENTION

Claim 46 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Hiraga in view of Pendse, as stated in the Office Action.

Claim 46 depend from independent claim 44, and thus include all the limitations of the independent claims from which it depends. Accordingly, as previously discussed with regard to claim 44 in issue C (pages 12-13), claim 46 are patentable over Hiraga in view of Pendse.

VIII. CONCLUSION

Appellant respectfully submits that all appealed claims in this application are patentable and were improperly rejected by the Examiner during prosecution before the United States Patent and Trademark Office. Appellant respectfully requests that the Board overrule the Examiner and direct allowance of the rejected claims.

This Brief is submitted with a check for $500.00 to cover the appeal fee for one other than a small entity as specified in 37 C.F.R. § 1.17(c). Please charge any shortages and credit any overpayments to our Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: March 24, 2006

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IX. APPENDIX OF CLAIMS (37 C.F.R. § 41.37(c)(1)(viii))

The claims on appeal read as follows:

1. A semiconductor device, comprising:

a die having

a first edge;

a core;

a plurality of bond pads configured in a staggered array between the first edge and the core, wherein the staggered array includes an inner ring and an outer ring of bond pads;

a first plurality of driver cells located between the first edge and the plurality of bond pads; and

a second plurality of driver cells located between the plurality of bond pads and the core.

3. The semiconductor device of claim 1, further comprising a plurality of pre-drive cells located between the second plurality of driver cells and the core.

5. The semiconductor device of claim 1, further comprising a plurality of metal connections, each of the plurality of metal connections to couple one of the first and second pluralities of driver cells to one of the plurality of bond pads.

6. The semiconductor device of claim 5, further comprising a plurality of conductive interconnects, each of the plurality of pre-driver cells coupled to one of the first and second pluralities of driver cells by at least one of the plurality of conductive interconnects.

7. The semiconductor device of claim 6, wherein each of the plurality of conductive interconnects are more narrow in width than each of the plurality of metal connections.

8. The semiconductor device of claim 7, wherein the first and second pluralities of driver cells each have a width of approximately 80 microns.

23. The semiconductor device of claim 6, wherein each of the conductive interconnects coupling a pre-driver cell to one of the first and second driver cells has a width ranging from approximately 1-2 microns.

24. The semiconductor device of claim 6, wherein at least one pre-driver cell is coupled to one of the first and second driver cells via multiple conductive interconnects.

25. The semiconductor device of claim 6, wherein at least one conductive interconnect is disposed on a layer other than a layer where the bond pads are disposed.

26. The semiconductor device of claim 25, wherein at least one conductive interconnect is disposed on different layer underneath at least one bond pad.

27. The semiconductor device of claim 25, wherein at least one conductive interconnect is disposed on different layer underneath at least one driver cell.

35. A semiconductor device, comprising:

a die having

a first edge;

a core;

a plurality of bond pads configured in an array between the first edge and the core;

a first plurality of driver cells located between the first edge and the plurality of bond pads;

a second plurality of driver cells located between the plurality of bond pads and the core; and

a plurality of conductive interconnects to couple each of a plurality of pre-driver cells to one of the first and second pluralities of driver cells, wherein at least one conductive interconnects is disposed on a layer other than a layer where the plurality of bond pads are disposed.

36. The semiconductor device of claim 35, wherein the plurality of bond pads are configured in a staggered array.

37. The semiconductor device of claim 36, wherein the plurality of pre-drive cells are located between the second plurality of driver cells and the core.

38. The semiconductor device of claim 37, wherein the plurality of bond pads configured in the staggered array include an inner ring and an outer ring of bond pads.

39. The semiconductor device of claim 38, further comprising a plurality of metal connections, each of the plurality of metal connections to couple one of the first and second pluralities of driver cells to one of the plurality of bond pads.

40. The semiconductor device of claim 39, wherein each of the plurality of metal connections to couple one of the first and second driver cells to one of the bond pads has a width that is approximately up to 80 microns.

41. The semiconductor device of claim 39, wherein each of the first driver cells is coupled to one of the outer ring of bond pads via one of the metal connections.

42. The semiconductor device of claim 41, wherein each of the second driver cells is coupled to one of the inner ring of bond pads via one of the metal connections.

43. The semiconductor device of claim 39, wherein at least one metal connection coupling a bond pad and a driver cell has a width equivalent to a width of one of the respective bond pad and the driver cell.

44. A system comprising:

a lead frame; and

a die coupled to the lead frame, the die having

a first edge,

a core,

a plurality of bond pads configured in a staggered array between the first edge and the core, wherein the staggered array includes an inner ring and an outer ring of bond pads,

a first plurality of driver cells located between the first edge and the plurality of bond pads, and

a second plurality of driver cells located between the plurality of bond pads and the core.

45. The system of claim 44, further comprising a plurality of pre-drive cells located between the second plurality of driver cells and the core.

46. The system of claim 45, wherein at least one of the first and second driver cells is a ESD (electrostatic discharge) cell.

47. The system of claim 46, wherein each of the driver cells provides at least one of a drive strength, reception of incoming signals, and ESD protection of the core.

48. The system of claim 47, wherein each of the pre-drive cells provides communication between the core and one or more driver cells.

X. EVIDENCE APPENDIX

None.

XI. RELATED PROCEEDINGS APPENDIX

None.

03-28-06

AF
RFW

TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application No.	09/475,643
Filing Date	December 30, 1999
First Named Inventor	Michael A. Jassowski
Art Unit	2891
Examiner Name	Zarneke, David A.
Total Number of Pages in This Submission	31
Attorney Docket Number	42390P7143

ENCLOSURES ***(check all that apply)***

- ☐ Fee Transmittal Form
  - ☐ Fee Attached
- ☐ Amendment / Response
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
  - ☐ PTO/SB/08
- ☐ Certified Copy of Priority Document(s)
- ☐ Response to Missing Parts/ Incomplete Application
  - ☐ Basic Filing Fee
  - ☐ Declaration/POA
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- ☐ Licensing-related Papers
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- ☐ Petition to Convert a Provisional Application
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- ☐ Proprietary Information
- ☐ Status Letter
- ☒ Other Enclosure(s) *(please identify below):*

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Remarks

- First Class Certificate of Mailing; - return reciept postcard;
- Response to Notice of Non-Compliant Appeal Brief; and
- an amended Appeal Brief to replace the the Appeal Brief submitted on January 12, 2006.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm *or* Individual name	Aslam A. Jaffery, Reg. No. 51,841 BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Signature	
Date	March 24, 2006

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I hereby certify that this correspondence is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Mail Stop Appeal Brief-Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Typed or printed name	Krista Mathieson		
Signature	Krista Mathieson	Date	March 24, 2006

Based on PTO/SB/21 (09-04) as modified by Blakely, Sokoloff, Taylor & Zafman (wlr) 11/30/2005.
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